GIVERNyLABS

Frequency Synthesizer & Jitter Cleaner Board featuring the TI-LMK04805, SI-569 and ATSAMD51 IC's

DESCRIPTION

A really fantastic trio: one of the best jitter cleaner and clock distributor (LMK04805) combined with one of the best voltage controlled frequency oscillator (SI-569). The best: Both can be flexibly programmed and steered with a SAMD51 Cortex M4 processor.

And because the board is Arduino compatible, the Board is easy to configurate and even better applications based on it can be developed very easily on the fly.

This board is software compatible with the Adafruit Metro M4 and it is powered with an ATSAMD51J19.

This board can be used as a frequency synthesizer and for clock distribution: 12 outputs can be flexibly configured and mixed with one another with regard to the format (LVCMOS, LVDS and LVPECL) and the output frequency. The frequency synthesizer is powered by a precise, ultra low jitter oscillator, the frequency of which can be programmed. The frequency of the oscillator is made available directly via 2 additional outputs. The board also has 2 frequency inputs for jitter cleaning. This means that these input frequencies can be cleaned of jitter and made available flexibly as an ultra low jitter signal via the frequency synthesizer. You can find a configuration example below in the document.

The Texas Instruments LMK04805 is one of the industry's highest performance clock conditioner with superior clock jitter cleaning, generation and distribution with advanced features to meet advanced system requirements. The dual loop architecture consists of two high performance phase-locked loops (PLL) and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides low-noise jitter cleaner functionality while the second PLL (PLL2) performs the clock generation and distribution. When used with a very narrow loop bandwidth, the PLL1 uses the superior close in phase noise of the SI-569 VCXO to clean one of the two selectable input clocks.

The LMK04805 is powered by a low noise SI-569 VCXO voltage controlled frequency oscillator. The Silicon Laboratories' Si569 Ultra Series utilizes advanced 4th generation DSPLL® technology to provide an ultra-low jitter (105 fs), low phase noise clock at any output frequency. The device is user-programmed via simple commands to provide for the LMK04805 any suitable frequency with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. The frequency oscillator offers excellent reliability and frequency stability as well as guaranteed aging performance.

In addition you can use the Clock & Jitter Cleaner Board as an I2C appliance to front end any microcomputer, e.g. the raspberry with clock, frequency synthesizer, clock distribution and jitter cleaning application capabilities.

The board is native USB, there's no need for a hardware USB to Serial converter as the board has built in USB support. When used to act like a serial device, the USB interface can be used by any computer to listen/send data to the board and can also be used to launch and update code via the bootloader.

- Output Clock Rates of up to 1536 MHz (LVDS, LVPECL), 250Mhz (LVCMOS)
- 7 differential / 14 single ended LVPECL, LVDS, LVCMOS programmable Output Clocks
- Digital Delay: fixed or dynamically adjustable
- Analog Delay: 25 ps step control
- 0-Delay Mode
- Clock Output Synchronization
- Holdover capability
- 2 differential / single ended Input Clocks for jitter cleaning
- Input clock with loss of signal detection
- Flexible Multi-Mode Configuration: Dual PLL, Single PLL and Clock Distribution
- Programmable to output frequencies from 0.002 to 1536 MHz
- Fast VXCO frequency adjustments on the fly over a range of +/- 950 ppm (parts-per-million) with 0.0001164 ppm resolution (continuous glitchless output)
- VCXO Temperature stability ±20 ppm (-40 to 85 °C)
- VCXO Total stability ±50 ppm (includes temperature stability, initial accuracy, load pulling, VDD variation and 20 year aging at 70 °C)
- Excellent PSNR and supply noise immunity
- 3.3V logic, 5V supply operation
- Cortex M4 core running at 120 MHz
- Floating point support with Cortex M4 DSP instructions
- 32-bit, 512 KB flash, 192 KB RAM
- Dual 1 MSPS DAC, dual 1 MSPS ADC (8 analog pins)
- 6 x hardware SERCOM (I2C, SPI or UART), 18 x PWM outputs
- SWD Interface
- USB Interface
- Built in crypto engines with AES (256 bit), true RNG, Pubkey controller
- Measures 4.96" x 3.64" x 0.28" (126mm x 92,5mm) without SMA connectors

Configuring the Clock & Jitter Cleaner Board via C/C++ code using the Arduino IDE

The board contains a fixed frequency crystal and a voltage controlled frequency synthesis IC using Silicon Labs patented DSPLLTM technology, enclosed in a standard hermetically sealed crystal oscillator package. The crystal provides the reference frequency used by the DSPLL frequency synthesis IC. The output frequency of the voltage controlled frequency oscillator (VCXO) can be dynamically set via register settings in the DSPLL frequency synthesis IC in order to provide the reference frequency for the PLL1 section of the LMK04805 dual loop architecture. Like the SI-569 the LMK04805 can be programmed via register settings using the Arduino IDE. The LMK04805 can be configured in a highly flexible manner and be operated in dual PLL, single PLL and clock distribution mode. The clock format, analog and digital delay can be freely chosen per output. This includes the clock divide value and the choice to select the source from either the LMK04805 VCO or the SI-569 VXCO.

Configuration example

The Frequency Synthesizer & Jitter Cleaner Board is used to remove jitter from two input LVCMOS frequencies:

- CLKIN0: 3.072 MHz
- CLKIN1: 6.144 MHZ

You can switch between the two input frequencies "on the fly". If the respective input frequency fails, the frequencies required at the output are still made available via the holdover function.

The oscillator feeding the frequency synthesizer and the jitter cleaner is programmed to 122.88 MHZ and the oscillator frequency is output at:

- OSCOUT0: 122.88 MHz, LVDS (differential positive)
- OSCOUT0*: 122.88 MHz, LVDS (differential negativ)

At the other outputs, the output frequency is ultra low jitter cleaned and synchronized with the input frequency in terms of phase and frequency shifts and provided with the following output frequencies and formats:

- CLKOUT0: 98.304 MHz, LVDS (differential positive)
- CLKOUT0*: 98.304 MHz, LVDS (differential negativ)
- CLKOUT2: 49.152 MHz, LVCMOS
- CLKOUT2*: Powerdown
- CLKOUT4: 12.288 MHz, LVCMOS
- CLKOUT4*: 12.288 MHz, LVCMOS (inverted)
- CLKOUT6: 6.144 MHz, LVCMOS
- CLKOUT6*: Powerdown
- CLKOUT8: 3.072 MHz, LVCMOS
- CLKOUT8*: 3.072 MHz, LVCMOS (inverted)
- CLKOUT10: 561.737 MHz, LVDS (differential positive)
- CLKOUT10*: 561.737 MHz, LVDS (differential negativ)

Consulting Services

Based on your wishes and requirements, we will be happy to advise you on the configuration and programming of the Frequency Synthesizer & Jitter Cleaner Board or create customer-specific hardware and software solutions.

We look forward to hearing from you at:

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